DIAMOND HILL

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Beyond Moore's Law: Semiconductor Industry at a Crossroads

Oct 2022

Gordon Moore, the co-founder of Intel, proposed the famous Moore's Law in 1965, which was a prediction that the number of transistors on a semiconductor chip would double about every two years. For over fifty years, Moore's Law has been the cornerstone of the semiconductor industry, and the pursuit of doubling transistor density every two years has enabled nearly everything in modern electronics from smartphones to the predictive power of data and artificial intelligence in massive data centers. Today, the latest Intel processors have nearly 3 billion transistors per chip, which is astonishing considering that processors in 1971 had 2,300 transistors. Additionally, the growth of the industry is impressive, surpassing $500 billion in sales in 2021.

Moore's law has had two main implications: economics and performance. As we shrink the size of semiconductor chip components, the manufacturing cost per component falls; smaller components are also faster and more efficient, translating into higher-performance chips both in terms of computational power and power consumption. For decades, the pursuit of miniaturization has enabled the improvement in economics and performance of semiconductor chips — however, now it seems that Moore's law is reaching its limits. The most advanced chips today are built by Taiwan Semiconductor Manufacturing Co. on 3 nanometer technology. To put that into perspective, 3 nanometers is the width of 60 hydrogen atoms or only about 15 silicon atoms. When we are trying to create features of such small sizes, the margin for error is significantly reduced. The manufacturing processes required to produce precision features on such small chips have become increasingly complex and expensive. In addition to cost and complexity, we are also approaching the physical limit where further shrinking might not even be possible.

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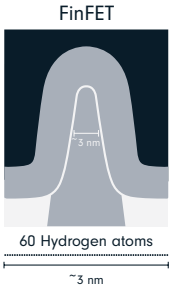

Miniaturization

Source: Entegris Company Presentation.

The rise in manufacturing complexity for the most advanced chips is already impacting the economics side of the Moore's law, as the industry no longer seems to be enjoying the kind of cost reductions previously experienced from shrinking chips. Dynamic random-access memory (DRAM) and NAND flash memory manufacturers have historically experienced over 20% declines in cost per bit per year but are now predicting only high-single digits declines in cost per bit going forward, and Taiwan Semiconductor has deviated from its past norm of reducing prices and instead raised prices by 10% to 20% over the last year across its processing technologies. Recently, graphics processing chip manufacturer Nvidia surprisingly announced significant price increases for its next-generation gaming chips with CEO Jensen Huan even saying in a press release that "Moore's Law is dead." More than ever before, it's increasingly clear that the economics of Moore's law are slowing down.

Although the economics are changing, current roadmaps from semiconductor equipment manufacturers show that it's possible to shrink chips to one to two nanometers over the next five to 10 years, albeit at a slower pace than in the past. Going forward, it might not be possible to shrink chips further using silicon as a base. Therefore, industry players will have to source alternative materials; research is underway in this regard but at this point it remains to be seen whether alternative materials will allow economically feasible chip shrinking to continue.

Another development we expect is that design and architecture will take precedence over size as shrinking becomes less feasible. One of the developments we have already seen is in the memory industry with 3D NAND architectures, which involves stacking numerous layers of memory cells over one another, thus allowing manufacturers to pack more memory within the same surface area. Additionally, memory manufacturers are also considering developing 3D DRAM memory.

We also expect advanced chip packaging and interconnects to allow for development of semiconductor products optimized for specific workloads. There are various advanced chip packaging techniques available which allow 3D stacking of chips or planar configuration of smaller chiplets. These packaging technologies mean the most advanced chips can be mixed with older chips, meaning the most advanced technologies are used only when needed. The design optimization from these packaging technologies can continue to enable performance benefits, power efficiency and in some cases cost benefits.

While the principles of Moore's law may be slowing down, we believe competition will continue to drive innovation through new design architectures, packaged chips optimized for specific workloads and ongoing research into alternative base materials. In the face of innovation and change, we continue to look for mispriced investment opportunities, and as distorted fundamentals normalize from their COVID peaks, we expect that market volatility will present us with more investment opportunities in this evolving space in the coming years.

As of 30 September 2022, Diamond Hill owned shares of Taiwan Semiconductor Manufacturing Co. Ltd.